A W-CDMA Zero-IF Front-End for UMTS in a 75 GHz SiGe BiCMOS Technology

Harald Pretl[1,2], Werner Schelmbauer[2], Linus Maurer[2], Hubert Westermayr[1], Robert Weigel[1,2]
Bernd-Ulrich Klepser[3], Bernd Adler[3], Josef Fenk[3]
[1]DICE Danube Integrated Circuit Engineering, Linz, Austria
[2]Institute for Communications and Information Engineering, University of Linz, Austria
[3]Infineon Technologies, Munich, Germany

Abstract — A zero-IF front-end consisting of an I/Q down-conversion mixer, broadband I/Q-generation, fully-integrated VCO, dual-modulus prescaler, low-noise baseband buffer and blocking filter is presented. Integrated in a 75 GHz f_t BiCMOS technology with 0.35 μm CMOS it draws 33 mA from a 2.7 V supply. Extremely low local-oscillator leakage of -95 dBm together with a high IIP2 of 55 dBm results in very low DC offset values of less than 20 mV at the baseband output of the IC. The presented circuit is intended for application in a highly-integrated UMTS receiver.

1. INTRODUCTION

Wideband wireless integrated circuits for UMTS transceivers will soon be put into production. Using W-CDMA technology for the air interface (called UTRA) data rates of up to 2 Mbit/s are possible for stationary and 384 kbit/s for mobile users [1]. The mode of UMTS that is put into operation first in Japan is frequency-division duplexing (FDD). Low-current consumption is thus an important feature for the user terminal equipment. A very high integration level for the radio part of the handset is another issue. The zero-IF (or direct-conversion) architecture is able to fulfill both requirements.

Recently, details about zero-IF receivers for W-CDMA have been published, both from academia ([2]) and industry ([3] and [4]), demonstrating the feasibility of this architecture.

The integrated circuit presented in this paper is going one step further by integrating the LO generation circuits (VCO and the prescaler as the high-frequency part of a complete phase-locked loop) together with the most critical analog building blocks, especially the I/Q down-conversion mixer and the baseband low-noise amplifier, onto one die to study coupling effects and performance as early as possible in the development cycle.

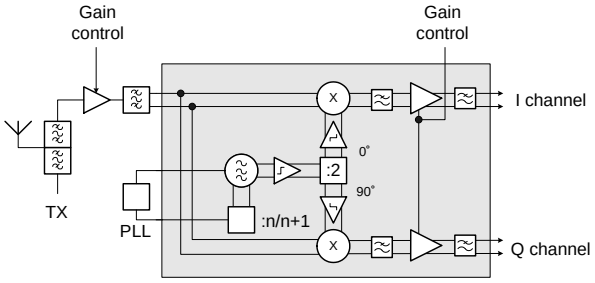

Figure 1: Block diagram of the UMTS zero-IF receiver for the FDD mode.

2. ZERO-IF FRONT-END

The block diagram of the UMTS zero-IF front-end for the FDD mode is shown in Fig. 1. After the antenna a duplexer filter attenuates the transmitter signal (TX) and provides out-of-band rejection for the receive signal. A low-noise amplifier (LNA) boosts the received signal to higher levels before an additional interstage surface-acoustic-wave (SAW) filter converts the single-ended signal into differential form [5]. This filter also relaxes the receiver requirements for IIP3 and IIP2 [6] due to a weaker transmitter signal at the input of the mixer [7].

The voltage-controlled oscillator (VCO) is fully-integrated and uses octagonal spiral inductors with

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thick top metal. It operates at the double receive frequency of 4220–4340 MHz (RX-band for FDD is 2110–2170 MHz) to reduce local-oscillator (LO) leakage and to enable broadband quadrature LO generation by frequency division using a master-slave toggle flip-flop. The LO path further includes driver stages for the LO signals to allow rapid switching of the differential pairs in the mixer core. The mixer is implemented as a standard Gilbert-cell type with differential RF inputs (easily matched to 100 Ω).

The dual-modulus prescaler is implemented in bipolar current-mode logic (CML) and is able to work up to 5 GHz with only 5.8 mA. It can be programmed to divide either by 32/33 or by 64/65. The divided signal is available outside the IC with CMOS compatible voltage levels.

The baseband part of the IC consists of a low-noise baseband buffer providing two gain settings (20 and −10 dB) followed by a low-pass filter of Butterworth type of 3^{rd} order. The nominal corner frequency of this blocking filter is set to 5 MHz.

Depending on the dynamic range of the analog-digital-converter (ADC) additional channel-selection and gain is required. Experience shows that implementing these functions is possible with low current consumption [8].

The IC is implemented in the Infineon Technologies B7HFc SiGe BiCMOS process. It features NPN bipolar transistors with f_t of 75 GHz and 0.35 μm CMOS. The circuit blocks are able to operate from a 2.7 V supply consuming about 33 mA. Temperature-independent biasing is achieved using a band-gap reference circuit. The IC includes ESD-protection at every pin. It is assembled in a plastic TQFP-48 package for evaluation.

3. Circuit Description

The mixer is a combination of the two structures that are presented in [9] and [2]: it features an NMOS common-gate differential input stage for a matched input together with a bipolar mixing quad for rapid switching with medium drive amplitude (Fig. 2). Two external inductors (10 nH each) are required for cancelling the capacitive part of the input impedance and for providing a DC-path to ground.

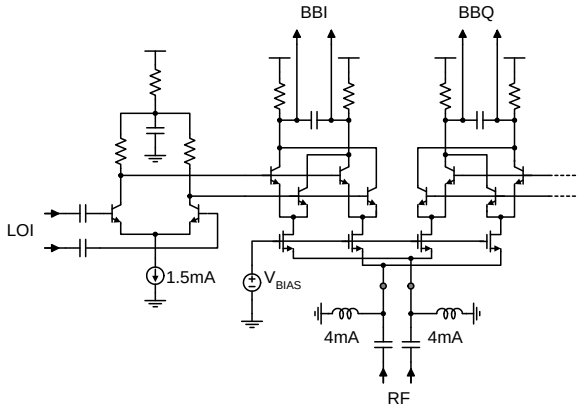

Figure 2: I/Q down-conversion mixer.

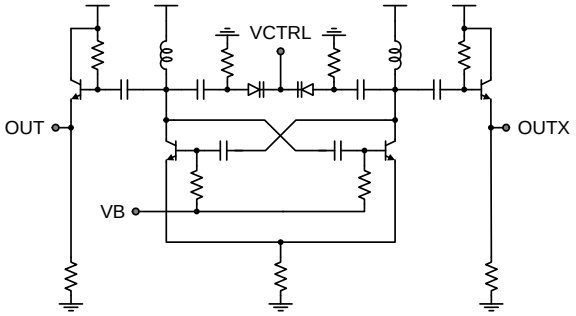

Figure 3: Fully-integrated VCO.

The excellent LO leakage of −95 dBm can be attributed to a very symmetrical layout using careful shielding and isolation techniques and the double-well BiCMOS technology. The integration of the VCO is also advantageous because the coupling of bond-wires is prevented. The matching of the transistors and resistors of the circuit is very critical to achieve high IIP2 values and low DC offsets. The typical values for this design are an IIP2 of 55 dBm and DC offset voltages of less than 20 mV at the baseband output (typically less than 2 mV at the output of the mixers). This design demonstrates that very good matching can be achieved by carefully selecting device dimensions and also carefully drawing the layout of the blocks using common-centroid techniques.

The VCO in Fig. 3 is similar to the structure

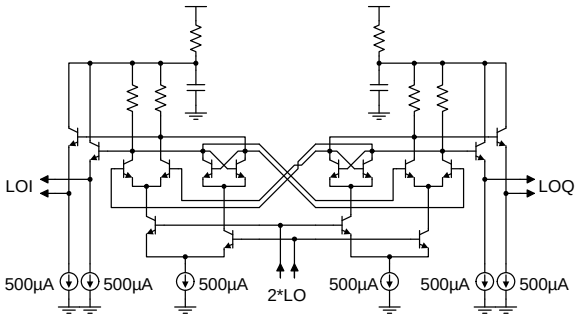

Figure 4: Frequency divider.

that was presented in [10]. It uses a bipolar cross-coupled differential pair with capacitive feedback. Weakly coupled emitter-followers isolate the VCO core from load pulling effects. The high quality factor Q of the integrated inductors built by using thick top metal translates into low current consumption when implementing a VCO with a nominal center frequency of 4.28 GHz. The phase noise requirements of UMTS are rather moderate due to the large channel spacing of 5 MHz, and additional 6 dB are gained by frequency dividing the VCO signal to produce the quadrature LO signals for the mixers. This frequency division using a master-slave toggle flip-flop can be realized with low current consumption (Fig. 4).

The dual gain-state low-noise baseband amplifier is implemented with two differently degenerated differential pairs in parallel. One of the two stages is active at a time, offering a good noise-linearity tradeoff.

The baseband amplifier is followed by a low-pass filter, called a blocking filter. This filter offers little adjacent-channel selectivity but attenuates blocking signals with larger frequency offsets. It is implemented as a Sallen-Key structure, and the passive pole of the filter is located at the output of the mixer. This passive pole provides selectivity at 10 and 20 MHz offset, thereby increasing the cascaded IIP3 of the front-end for the intermodulation test. Additionally, the transmitter signal at the duplex distance is attenuated heavily, so cross-modulation is negligible in the baseband chain of the receiver.

Table 1: Circuit performance (V_{CC}=2.7 V, 27 °C)

Parameter	**Simulated**	**Measured**
Mixer voltage gain	6 dB	
Baseband voltage gain	20 dB	
	−10 dB	
Mixer IIP3	14 dBm	13 dBm
Mixer DSB-NF	13 dB	
Mixer P_{1dB}	0 dBm	
VCO tuning (2 V)	10 %	
@ 0.4 V		3.9 GHz
@ 2.4 V		4.4 GHz
VCO phase-noise		
@ 100 kHz	−86 dBc/Hz	
I/Q phase error		2.5 °
Cascaded voltage gain		24.2 dB
		−3.7 dB
Cascaded IIP3		4 dBm
		13 dBm
DSB-NF (hi gain)		15 dB
Cascaded P_{1dB}		−24 dBm
		1 dBm
LO leakage		−95 dBm
IIP2 (hi and lo gain)		55 dBm
DC offset		10 mV
		20 mV
S_{11} (2×10 nH)		−13 dB

4. Measurement Results

For the measurements a 3-layer test-board was designed. The VCO is locked to a reference frequency using an external PLL and the internal prescaler. A phase-detector frequency of 400 kHz was used (a channel raster of 200 kHz is required in UMTS for compatibility to GSM). The doubling of the phase-detector frequency when using a VCO at the double receive frequency is another advantage of this approach, which is enabled by the fast low-power prescaler available in B7HFc. The bandwidth of the loop was set close to 40 kHz.

A rat-race coupler on a standard FR4 substrate was used for generating the balanced signals needed at the mixer input port. This micro-strip circuit features an insertion loss of 0.7 dB and a phase error of 3 ° in a frequency band of 2000–2200 MHz.

The differential baseband outputs are converted into single-ended outputs by discrete instrumental amplifiers with $50\,\Omega$ drive capability. Using this measurement setup the parameters summarized in Tab. 1 have been obtained.

5. Conclusion

The zero-IF architecture is very suitable for UMTS receivers. The very high level of integration offers the benefit of a small PCB area required for the radio transceiver, especially important for the design of a multi-standard handset. This implementation shows that a zero-IF receiver can be built with low current consumption (33 mA for the present IC) in a high-speed SiGe BiCMOS technology, which is important for a receiver for the FDD mode.

The most important parameters of this zero-IF receiver IC for the application in a W-CDMA system are: exceptionally low LO leakage of $-95\,$dBm, high IIP2 of 55 dBm and DC offset voltages of less than 20 mV. Adding a low-noise amplifier, channel-select filters and programmable gain amplifiers a complete receiver IC can be built which offers sufficient performance for the UMTS standard.

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